What is claimed is:

1. A sampling clock generation circuit which generates a sampling clock used for sampling data, the sampling clock generation circuit comprising:

an edge detection circuit detecting between which two edges a data edge is located, the two edges being among edges of first to N-th clocks having the same frequency but mutually different phases; and

a clock selection circuit which selects one clock from among the first to N-th clocks, based on detection information from the edge detection circuit, and outputs the selected clock as the sampling clock.

2. The sampling clock generation circuit as defined by claim 1,

wherein the edge detection circuit comprises:

a first holding circuit which holds data by using the first clock,... a J-th holding circuit which holds data by using a J-th clock (where: $1 < J < N$),... and an N-th holding circuit which holds data by using the N-th clock; and

a first detection circuit which detects whether or not there is a data edge between the edges of the first clock and a second clock, based on data held in the first holding circuit and a second holding circuit,... a J-th detection circuit which detects whether or not there is a data edge between the edges of the J-th clock and a (J + 1)-th clock, based on data held

in the J-th holding circuit and a (J + 1)-th holding circuit, ... and an N-th detection circuit which detects whether or not there is a data edge between the edges of the N-th clock and the first clock, based on data held in the N-th and first holding circuits, and

wherein the clock selection circuit selects a clock from among the first to N-th clocks, based on edge detection information from the first to N-th detection circuits, and outputs the selected clock as the sampling clock.

3. The sampling clock generation circuit as defined by claim 2,

wherein, when a set-up time of the first to N-th holding circuits is TS, a hold time of the first to N-th holding circuits is TH, and a period of each of the first to N-th clocks is T, number of clocks N of the first to N-th clocks is such that: $N \leqq [T/(TS + TH)]$ (where [X] is a maximum integer that does not exceed X).

4. The sampling clock generation circuit as defined by claim 3,

wherein number of clocks N is such that $N = [T/(TS + TH)]$ (where [X] is a maximum integer that does not exceed X).

5. The sampling clock generation circuit as defined by claim 1,

wherein the number of clocks N of the first to N-th clocks

is such that N = 5.

6. The sampling clock generation circuit as defined by claim 3,

wherein the number of clocks N of the first to N-th clocks is such that N = 5.

7. The sampling clock generation circuit as defined by claim 4,

wherein the number of clocks N of the first to N-th clocks is such that N = 5.

8. The sampling clock generation circuit as defined by claim 1,

wherein the clock selection circuit selects from the first to N-th clocks a clock having an edge that is shifted by a given set number M of edges from a data edge, and outputs the selected clock as the sampling clock.

9. The sampling clock generation circuit as defined by claim 8,

wherein the number M is set to a number that ensures a set-up time and a hold time of a circuit which holds data based on the generated sampling clock.

10. A sampling clock generation circuit which generates a sampling clock used for sampling data, the sampling clock

generation circuit comprising:

an edge detection circuit which detects a data edge; and

a clock selection circuit which selects a clock from among first to N-th clocks having the same frequency but mutually different phases, based on detection information from the edge detection circuit, and outputs the selected clock as the sampling clock,

wherein the edge detection circuit comprises at least one holding circuit which holds data at any clock from among the first to N-th clocks, and

wherein, when a set-up time of the holding circuit comprised by the edge detection circuit is TS, a hold time of the holding circuit comprised by the edge detection circuit is TH, and a period of each of the first to N-th clocks is T, number of clocks N of the first to N-th clocks is such that: $N \leqq [T/(TS + TH)]$ (where [X] is a maximum integer that does not exceed X).

11. The sampling clock generation circuit as defined by claim 10,

wherein number of clocks N is such that $N = [T/(TS + TH)]$ (where [X] is a maximum integer that does not exceed X).

12. The sampling clock generation circuit as defined by claim 10,

wherein the number of clocks N of the first to N-th clocks is such that N = 5.

13. The sampling clock generation circuit as defined by claim 11,

wherein the number of clocks N of the first to N-th clocks is such that N = 5.

14. A sampling clock generation circuit which generates a sampling clock used for sampling data, the sampling clock generation circuit comprising:

an edge detection circuit which detects a data edge; and

a clock selection circuit which selects a clock from among first to N-th clocks having the same frequency but mutually different phases, based on detection information from the edge detection circuit, and outputs the selected clock as the sampling clock,

wherein the clock selection circuit selects from the first to N-th clocks a clock having an edge that is shifted by a given set number M of edges from the data edge, and outputs the selected clock as the sampling clock.

15. The sampling clock generation circuit as defined by claim 14,

wherein the number M is set to a number that ensures a set-up time and a hold time of a circuit which holds data based on the generated sampling clock.

16. The sampling clock generation circuit as defined by claim 1, further comprising:

a PLL circuit having an oscillation circuit with a variably-controlled oscillation frequency, and phase-synchronizing a clock generated by the oscillation circuit with a base clock,

wherein the first to N-th clocks is generated based on outputs of first to N-th inversion circuits of an odd number of stages included in the oscillation circuit.

17. The sampling clock generation circuit as defined by claim 10, further comprising:

a PLL circuit having an oscillation circuit with a variably-controlled oscillation frequency, and phase-synchronizing a clock generated by the oscillation circuit with a base clock,

wherein the first to N-th clocks is generated based on outputs of first to N-th inversion circuits of an odd number of stages included in the oscillation circuit.

18. The sampling clock generation circuit as defined by claim 14, further comprising:

a PLL circuit having an oscillation circuit with a variably-controlled oscillation frequency, and phase-synchronizing a clock generated by the oscillation circuit with a base clock,

wherein the first to N-th clocks is generated based on outputs of first to N-th inversion circuits of an odd number of stages included in the oscillation circuit.

19. The sampling clock generation circuit as defined by claim 16,

wherein at least one of a disposition of the first to N-th inversion circuits and interconnection of output lines of the first to N-th inversion circuits is performed in such a manner that phase differences between the first to N-th clocks are equal.

20. The sampling clock generation circuit as defined by claim 17,

wherein at least one of a disposition of the first to N-th inversion circuits and interconnection of output lines of the first to N-th inversion circuits is performed in such a manner that phase differences between the first to N-th clocks are equal.

21. The sampling clock generation circuit as defined by claim 18,

wherein at least one of a disposition of the first to N-th inversion circuits and interconnection of output lines of the first to N-th inversion circuits is performed in such a manner that phase differences between the first to N-th clocks are equal.

22. The sampling clock generation circuit as defined by claim 16,

wherein lines for the first to N-th clocks are interconnected in such a manner that the parasitic capacitances of lines of the first to N-th clocks are equal.

23. The sampling clock generation circuit as defined by claim 17,

wherein lines for the first to N-th clocks are interconnected in such a manner that the parasitic capacitances of lines of the first to N-th clocks are equal.

24. The sampling clock generation circuit as defined by claim 18,

wherein lines for the first to N-th clocks are interconnected in such a manner that the parasitic capacitances of the lines of the first to N-th clocks are equal.

25. A data transfer control device for providing data transfer over a bus, the data transfer control device comprising:

the sampling clock generation circuit as defined by claim 1; and

a circuit which holds data, based on the sampling clock generated by the sampling clock generation circuit, and performs given processing for data transfer, based on the held data.

26. A data transfer control device for providing data

transfer over a bus, the data transfer control device comprising:

the sampling clock generation circuit as defined by claim 10; and

a circuit which holds data, based on the sampling clock generated by the sampling clock generation circuit, and performs given processing for data transfer, based on the held data.

27. A data transfer control device for providing data transfer over a bus, the data transfer control device comprising:

the sampling clock generation circuit as defined by claim 14; and

a circuit which holds data, based on the sampling clock generated by the sampling clock generation circuit, and performs given processing for data transfer, based on the held data.

28. The data transfer control device as defined by claim 25, wherein data transfer is in accordance with the Universal Serial Bus (USB) standard.

29. The data transfer control device as defined by claim 26, wherein data transfer is in accordance with the Universal Serial Bus (USB) standard.

30. The data transfer control device as defined by claim 27, wherein data transfer is in accordance with the Universal Serial Bus (USB) standard.

31. Electronic equipment comprising:

the data transfer control device as defined by claim 25; and

a device which performs output processing, fetch processing or storage processing on data transferred through the data transfer control device and the bus.

32. Electronic equipment comprising:

the data transfer control device as defined by claim 26; and

a device which performs output processing, fetch processing or storage processing on data transferred through the data transfer control device and the bus.

33. Electronic equipment comprising:

the data transfer control device as defined by claim 27; and

a device which performs output processing, fetch processing or storage processing on data transferred through the data transfer control device and the bus.

34. Electronic equipment comprising:

the data transfer control device as defined by claim 28;

and

a device which performs output processing, fetch processing or storage processing on data transferred through the data transfer control device and the bus.

35. Electronic equipment comprising:

the data transfer control device as defined by claim 29; and

a device which performs output processing, fetch processing or storage processing on data transferred through the data transfer control device and the bus.

36. Electronic equipment comprising:

the data transfer control device as defined by claim 30; and

a device which performs output processing, fetch processing or storage processing on data transferred through the data transfer control device and the bus.